AF/C# 2815

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ATTORNEYS AT LAW

Docket No.: 212812US-2

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: Application Serial No.: 09/930,202
Applicants: Takashi Ipposhi, et al.
Filing Date: August 16, 2001
For: SEMICONDUCTOR WAFER
Group Art Unit: 2815
Examiner: NGUYEN, J.

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF (IN TRIPLICATE)

Our check in the amount of **$320.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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212812US-2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

TAKASHI IPPOSHI ETAL. : GROUP ART UNIT: 2815

SERIAL NO: 09/930,202 : EXAMINER: JOSEPH NGUYEN

FILED: AUGUST 16, 2001 :

FOR: SEMICONDUCTOR WAFER

APPEAL BRIEF

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Please consider Appellants' arguments on appeal as provided below.

I. Real Party in Interest

The real party in interest is Mitsubishi Denki Kabushiki Kaisha.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-10 are active in this case. Claims 1-10 stand finally rejected.

IV. Status of Amendments

No amendments were filed subsequent to the final action dated September 30, 2002.

V. Summary of Invention

The present invention provides a semiconductor wafer 100 including first and second semiconductor wafers 1 and 3, respectively, having crystal orientation display sections 1a and

3a, respectively, indicative of crystal orientations formed thereon. See Figure 1. The first and second semiconductor wafers are bonded with the crystal orientation display sections shifted from one another. See Figure 1 and page 13 line 20 – page 14 line 3 of the written description. A second embodiment provides printing (e.g., LOT No. 009) which is provided on an exposed part of the main surface of the semiconductor wafer. See Figure 3.

VI. Issues

Whether claims 1, 4, and 5-8 are unpatentable under 35 USC 103(a) over the Appellants admitted prior art in view of US patent No. 5,060,043 to Yasue.

VII. Grouping of Claims

The claims of the group do not stand or fall together. Appellants submit that the claims should be grouped as shown below.

Group 1: Claims 1-4 and 8-10

Group 2: Claims 5-7

VIII. Argument

A. Introduction

The claims of group 1 and 2 should be considered separately because the inventions defined by the two groups of claims are separately patentable. The claims of group 1 define a semiconductor wafer including first and second semiconductor wafers having crystal orientation display sections indicative of crystal orientations formed thereon. The first and second semiconductor wafers are bonded with the crystal orientation display sections shifted from one another. In contradistinction thereto, the claims of group 2 define a semiconductor wafer including first and second semiconductor wafers wherein the first and second wafers are bonded in such a manner that a part of the main surface of the first semiconductor wafer is

exposed because the crystal orientation display section of the second wafer is configured to expose that part of the main surface. Printing is provided on the exposed part of the wafer.

Appellants respectfully submit that configuration of the crystal display section of the second wafer such that it enables printing on the first wafer would have been non-obvious in view of the subject matter defined by the first group of claims.

B. Group 1

The September 30, 2002 final action states with regard to Claims 1, 5 and, 8 that:

> With respect to claims 1, 5, 8, applicant argues that either (APA) or Yasue teaches or suggests the "shifting" limitation in claim 1. However, by combining (APA) and Yasue in which figure 17 of (APA) is modified with nicks indicative of crystal orientations formed on fringes from Yasue (figure 1), the first and second semiconductor wafers of (APA) are bonded with said crystal orientation display section would be shifted each other. That is, it would make sense to have additional nick (notch) formed on the surface other than the surface on which the notch 1a (figure 17 of APA) is already formed, and thereby the first and second semiconductor wafers of (APA) would be shifted each other in a similar manner as figure 1 of the present application.

Appellants submit that neither the (APA) or Yasue teach or suggest the shifting feature defined by the claims of group 1. That is, Figure 1 of Yasue merely discloses a single wafer including crystal orientation marks and Appellants' Figure 17 illustrates two wafers where the orientation marks are unshifted. Hence, Appellants submit that even when combined the structures illustrated in the two figures would not have rendered obvious the subject matter defined by the claims of group 1.

Furthermore, neither the (APA), Yasue, or the final action provide a motivation to combine the disclosed structures. The office action merely states that "it would make sense to have additional nick" but does not offer a reason why it would make sense. Consequently, the (APA) is not believed to anticipate or render obvious the invention defined by the claims of

group 1 when considered alone or in combination with Yasue.

C. Group 2

The final action asserts with regard to claim 5 that the "APA" discloses "printing ... given to said part of said main surface of said semiconductor wafer." Appellants strongly disagree with that assertion. None of the figures identified as prior art by Appellants disclose such a feature. Compare Figures 3 and 4 with Figures 17-21. Further, none of the applied patents and/or publications teach or suggest such a feature. Hence, the subject matter defined by the claims of group 2 is believed to be allowable.

Respectfully submitted,

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IX. Appendix

1. A semiconductor wafer comprising:

first and second semiconductor wafers having crystal orientation display sections to be nicks indicative of crystal orientations formed on fringes thereof,

wherein said crystal orientation display sections are indicative of an identical crystal orientation in said first and second semiconductor wafers, and

said first and second semiconductor wafers are bonded with said crystal orientation display sections shifted from each other.

2. The semiconductor wafer according to claim 1, wherein both of said first and second semiconductor wafers are (100) wafers in which (100) planes are main surfaces, and

said crystal orientation display sections are shifted from each other by 45 degrees or 135 degrees.

3. The semiconductor wafer according to claim 2, wherein said first semiconductor wafer is a wafer for a support substrate and said second semiconductor wafer is a wafer for a device formation, and

a main surface of said wafer for the device formation is provided with a semiconductor device including a MOS transistor in which a channel direction between a source and a drain is parallel with a direction of a crystal orientation <100>.

4. The semiconductor wafer according to claim 1, wherein said first semiconductor wafer is a wafer for a support substrate,

said second semiconductor wafer is a wafer for an SOI layer, and

an insulating film is formed on a main surface of at least one of said wafer for the support substrate and said wafer for the SOI layer.

5. A semiconductor wafer comprising:

a first semiconductor wafer; and

a second semiconductor wafer having a crystal orientation display section to be a nick indicative of a crystal orientation formed on a fringe,

wherein said first and second semiconductor wafers are bonded to each other such that a part of a main surface of said first semiconductor wafer is exposed to said crystal orientation display section of said second semiconductor wafer, and

printing is provided to said part of said main surface of said first semiconductor wafer.

6. The semiconductor wafer according to claim 5, wherein a crystal orientation display section to be a nick indicative of a crystal orientation is also formed on a fringe of said first semiconductor wafer, and

said crystal orientation display section of said first semiconductor wafer and said crystal orientation display section of said second semiconductor wafer form an angle.

7. The semiconductor wafer according to claim 5, wherein said first semiconductor wafer is a wafer for a support substrate,

said second semiconductor wafer is a wafer for an SOI layer, and

an insulating film is formed on a main surface of at least one of said wafer for the support substrate and said wafer for the SOI layer.

8. A semiconductor wafer comprising:

first and second semiconductor wafers having bulk structures,

wherein said first and second semiconductor wafers are bonded with crystal orientations shifted from each other.

9. The semiconductor wafer according to claim 8, wherein both of said first and second semiconductor wafers are (100) wafers in which (100) planes are main surfaces, and

said crystal orientations are shifted from each other by 45 degrees or 135 degrees.

10. The semiconductor wafer according to claim 9, wherein said first semiconductor wafer is a wafer for a support substrate and said second semiconductor wafer is a wafer for a device formation, and

a main surface of said wafer for the device formation is provided with a semiconductor device including a MOS transistor in which a channel direction between a source and a drain is parallel with a direction of a crystal orientation <100>.